how to design broadband jfet amplifiers to provide top performance from VLF to over 100 MHz

A discussion of broadband jfet amplifier design, with special emphasis on IMD performance and matching

Broadband rf amplifiers are becoming increasingly useful in hf/vhf receiving applications. A modern wideband upconverting high-frequency receiver, for example, often employs a broadband rf amplifier as the first active stage. The rf stage improves the receiver noise figure and reduces undesirable LO-to-antenna conduction. Broadband amplifiers are also useful in a wide variety of other Amateur applications ranging from antenna preamplifiers to home-constructed test equipment. This article deals with some of the considerations involved in the design and construction of broadband jfet rf amplifiers. The circuits presented can be easily duplicated with readily obtainable components.

Other than to provide selectivity, a broadband rf amplifier must do everything that a narrowband amplifier does. Thus gain, noise figure, stability, and most other parameters must be comparable. There is, however, a major additional requirement. Since the broadband amplifier responds to signals over a very wide bandwidth, it is important that the amplifier have exceptionally high resistance to overload and intermodulation distortion (IMD).

With respect to overload, there are potentially many more signals over the larger bandwidth (in comparison with a narrowband amplifier) that might drive the amplifier into its gain compression (overload) region. With respect to IMD, there are many more combinations of frequencies at which these strong signals can cause the amplifier to produce intermodulation products that could interfere with

By Alex Burwasser, N6DC, 5022 Artesian Street, San Diego, California 92117

signals we are trying to receive. The intermodulation problem is compounded by the fact that unlike the narrowband amplifier, which is vulnerable only to odd-order IMD, both odd- and even-order IMD can produce interfering intermodulation products in the broadband amplifier. The narrowband amplifier is relatively immune to second-order IMD because its bandwidth is much less than an octave. Within this sub-octave bandwidth, there is no combination of frequencies at which in-band signals can produce second-order intermodulation products that also fall in-band (that is, second-order intermodulation products that are capable of interfering with in-band signals we might be trying to receive).[1,2]

Thus, in broadband receivers, it is very important to employ rf amplifiers that have extremely high resistance to both odd- and even-order IMD. These same considerations also apply to mixers.

broadband jfet amplifier

When considering an active device to be employed as a broadband amplifier, you must look for certain qualities. High transconductance is desirable. Input, output, and feedback capacitances should be low. The device should exhibit good noise performance and high signal handling capability.

High-quality jfets satisfy all of these requirements (with the exception of low feedback capacitance)

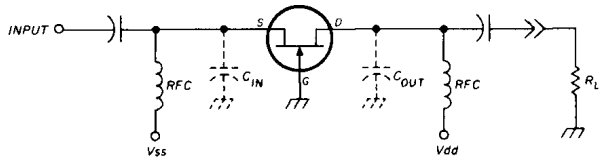

fig. 1. Schematic diagram of the simplified grounded-gate jfet amplifier.

reasonably well. By operating a jfet in the grounded-gate configuration, you can effectively reduce its otherwise high feedback capacitance to a very low level. Earlier, I mentioned that one of the desirable features of rf amplifiers in receivers is reverse isolation, or more specifically, the amplifier's ability to attenuate LO energy from the mixer to the antenna. The grounded-gate/base/grid configuration yields the best reverse isolation of any of the three possible amplifier configurations.

A simplified circuit of a grounded-gate jfet amplifier is shown in **fig. 1**. You can gain some insight into the operation of this circuit by applying some fundamental (and somewhat simplified) relationships. A more general and rigorous presentation of these relationships may be found in reference 3. The first relationship defines the input impedance of the amplifier. Disregarding the imaginary (reactive) component, the approximate input impedance is given by the expression:

$$R_{in} \approx \frac{1}{G_m} \quad (1)$$

where R_{in} is the real component of the input impedance and G_m is the device transconductance. A grounded-gate jfet with a transconductance of 10,000 micromhos, for example, would have an approximate input impedance of 100 ohms.

The second relationship defines the voltage gain of the amplifier. This relationship is:

$$A_v \approx G_m \times R_L \quad (2)$$

where A_v is the voltage gain

G_m is the device transconductance

R_L is the load resistance

Rearranging **eq. 1** to solve for G_m produces:

$$G_M \approx \frac{1}{R_{in}} \quad (3)$$

and substituting this expression of G_m into **eq. 2** produces:

$$A_v \approx \frac{R_L}{R_{in}} \quad (4)$$

That is, the approximate voltage gain is simply the ratio of the load resistance to the device input impedance.

Referring back to **fig. 1**, observe that the driving source, the jfet, and the load are all in series. Disregarding the input and output capacitances for the moment, it is evident then that the current gain, A_i, of this amplifier must be equal to unity because the current in a series circuit is everywhere the same. Power gain, A_p, is given by the expression

$$A_p = A_v \times A_i \quad (5)$$

Since A_i equals unity in a grounded-gate jfet amplifier, then

$$A_p = A_v \quad (6)$$

In other words, the power gain equals the voltage gain.

It would seem then that to obtain high power gain out of this amplifier, all that is necessary is to make R_L large. This is true up to a point, but even if you disregard the inherent output conductance of the jfet (which could be represented as an equivalent conductance from the drain to the source), you would find that C_{out} (the jfet output capacitance) would limit the output impedance and device gain at high

frequencies. Assuming a constant transconductance over the frequency range of interest, and disregarding C_{in},

$$f_{3dB} \approx \frac{1}{2\pi R_L C_{out}} \quad (7)$$

where f_{3dB} is the high-end frequency at which the amplifier gain is 3 dB down from its low frequency value.

To obtain the widest bandwidth, then, **eq. 7** indicates that you should employ a jfet with a very low output capacitance driving a low value of R_L. You can arbitrarily select a low value for R_L, but to maintain high power gain, **eq. 4** says that you will need a low value of R_{in} (the jfet input impedance). However, since $R_{in} = 1/G_m$ from **eq. 1**, this is actually just another way of saying that you need a jfet with high transconductance.

Given the above, it is evident that a useful figure of merit for a jfet in broadband operation is the ratio of device transconductance to output capacitance. A jfet with an exceptionally high transconductance to output capacitance ratio is the Siliconix U310.[4]

U310s are rather expensive, but a plastic economy version (the J310) is also available with performance characteristics that are substantially the same. The J310 is manufactured by Siliconix and National Semiconductor. Siliconix also offers a matched pair of J310-type jfets in an epoxy package. This device is the E430.

By the time this article is published, the E430, in all probability will have been phased out in favor of the U430. The U430 will employ the same chip geometry as the E430, but will use an 8-pin metal package similar to the TO-5 package.

The J310 is described in the *Siliconix FET Data Book*[5] as a low-noise, wide-dynamic-range device capable of high power gain at frequencies up to at least 450 MHz. The typical transconductance is listed at 12,000 micromhos at a drain current of 10 mA. The amplifiers presented in this article employ J310s and E430s.

The input impedance of a J310 or E430 grounded-gate amplifier can be made close enough to 50 ohms so that a reasonable input VSWR can be achieved without any matching network. The signal can simply be capacitively coupled to the jfet source. The disadvantage of this convenient technique is that the input impedance may not be optimum for best noise figure.

As previously mentioned, the load impedance (R_L) must be high compared with the jfet input impedance to obtain high power gain. Since the required value of R_L is much higher than the assumed 50-ohm load the amplifier is ultimately driving, broadband autotransformers can be employed to convert the 50-ohm load impedance to the higher level of R_L required to achieve reasonable gain in the jfet amplifier. Fifty ohms is selected as the desired ultimate load impedance since this is the nominal impedance level of most broadband mixers that might follow the amplifier.

jfet biasing

In biasing a jfet, there are three general requirements. The first is that the jfet maintain the desired bias current level over the anticipated temperature range. The second requirement is that the biasing circuit should not be device-sensitive. That is, if you design an amplifier employing a J310 biased at 18 mA of drain current, this drain current should be close to 18 mA for *any* J310. The third requirement is that the bias current should be insensitive to changes in supply voltages.

The first requirement is not too difficult to meet. Even with a poor biasing circuit, the bias current will remain fairly constant over a reasonably wide temperature range.

The second requirement can be relaxed somewhat where repeatability isn't so important. Since Amateur home projects are usually built in very small quantities, there is no particular problem with using pot or selecting resistors to achieve the desired bias current (especially if doing so permits the use of simpler circuitry or reduces power consumption).

The third requirement is also easy to meet. If the jfet is operated from a single supply voltage (V_{dd}), the inherent constant-current characteristics of the jfet will automatically stabilize the bias current, provided that the drain-to-source voltage is at least 6 volts or so (depending upon the particular jfet). If the jfet is supplied by both positive and negative voltages (V_{dd} and V_{ss}, respectively), the bias current may be somewhat sensitive to changes in V_{ss}. However, the situations where dual supply voltages are available will also be the situations where these supplies are *most likely to be regulated.*

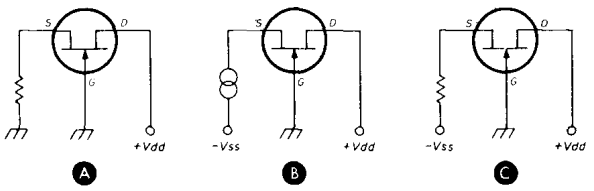

fig. 2. Diagrams of the three jfet biasing configurations with only the relevant dc circuitry shown. Schematic (A) shows the simplest, and poorest, configuration. The circuit is very device-sensitive, in that it is necessary to select the bias resistor for the desired current. Diagram (B) illustrates the use of a constant-current source to bias the jfet. The best overall compromise is shown in (C), where a negative voltage and large-value resistor act as a pseudo constant-current source.

Fig. 2 illustrates three commonly used jfet biasing circuits. For simplicity, only the relevant dc circuitry is shown. **Fig. 2A** shows the most commonly used (and poorest) jfet biasing configuration. Although its performance over a temperature range is adequate in most cases, it tends to be very device-sensitive. It is therefore necessary to select the resistor (or make it variable) to secure the desired bias current. On the plus side, overall power consumption is lower than that of the other two configurations and no negative supply is required. In **fig. 2B**, the jfet is biased by a constant-current source. If the constant-current source (usually a bipolar transistor with a temperature compensating diode) is temperature stable, this biasing scheme is nearly impervious to temperature, device, and supply voltage variations, and is thus an excellent biasing configuration.

A compromise configuration is shown in **fig. 2C**. This circuit is very similar to that of **fig. 2A** except that the resistor is larger and is returned to a negative supply. The negative voltage and large resistance act as a pseudo constant-current source. The larger value of the resistor and the magnitude of V_{SS}, the closer this biasing circuit comes to approximating a true constant-current source. If the negative voltage supply is available, this circuit offers the best performance for the number of components required. Temperature stability is very good, and the circuit is reasonably insensitive to device variations. As a brute-force test, this circuit was constructed with a J310 biased at a nominal current level of 18 mA using ± 12 volt supplies. Ten different J310s were tried in the circuit. The measured bias currents were all well within a 10 per cent window. Heating the devices for 10 seconds by applying a 25-watt soldering iron of less than 10 per cent. Similarly, chilling the devices with an aerosol spray coolant for a period of 10 seconds also resulted in a bias current change of less than 10 per cent.

Although the amplifiers described in this article all employ the biasing configuration of **fig. 2C**, substanany of these bias configurations. More detailed information on the subject of jfet biasing can be found in reference (3).

basic jfet broadband amplifier

Fig. 3A shows a simple broadband amplifier. Although this circuit is presented primarily for purposes of illustration, it nonetheless has many practical applications. The circuit is a grounded-gate jfet amplifier employing a single J310 biased at 18 mA of drain current. The output employs a peaking inductor and a 4:1 bifilardwound auto-transformer (detailed winding information is presented later in this article). The peaking inductor extends the frequency response. **Fig. 3B** shows the frequency response when L_1 is set for optimum gain flatness with respect to frequency. The setting of L_1 is not particularly critical, although it does substantially affect the high-end frequency response. Other performance characteristics are as follows:

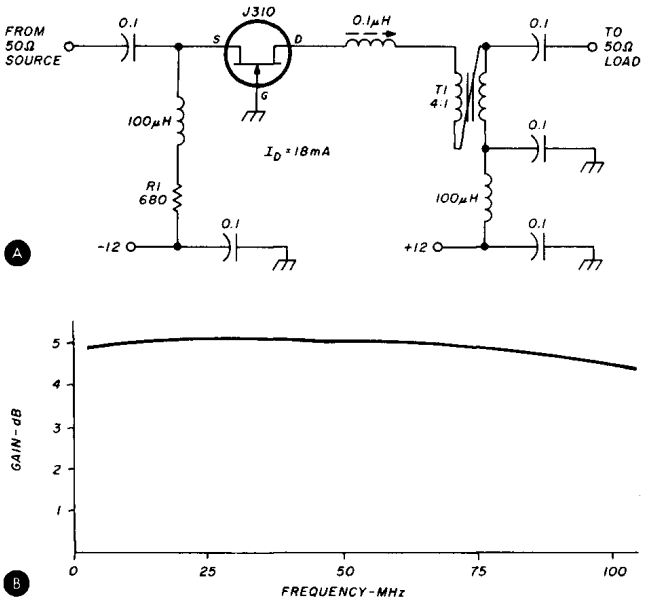

fig. 3. Schematic diagram of the basic broadband jfet amplifier. R1 sets I_D at 18 mA. (B) shows the frequency response of this basic amplifier.

1 dB gain compression level	+ 13 dBm
2nd-order intercept point	+ 28 dBm
3rd-order intercept point	+ 22 dBm
30-MHz noise figure	4.5 dB
input VSWR	1.3:1 from 1.8-100 MHz
reverse isolation	38 dB or better to 30 MHz; 25 dB or better to 200 MHz

The intermodulation and overload specifications for all amplifiers presented in this article are referenced to the amplifier input. The + 13 dBm specification for the 1 dB gain compression level, for example, is the *input* (rather than output) level at which 1 dB of gain compression occurs. When evaluating the intermodulation and overload performance of a device, it's very important to know whether the specifications are referenced to the input or output. Unfortunately, many manufacturers specify their devices without providing information as to whether the specification ferred method is to reference the specification to the input.

The output referenced specification is simply the input referenced specification plus the device gain. For example, an amplifier having an input referenced 3rd-order intercept point of + 20 dBm and a gain of 10 dB has an output referenced 3rd-order intercept point of + 30 dBm.

Some clarification is in order concerning this amplifier. First, the good input VSWR trades off against optimum noise figure. With a 1:1 input VSWR

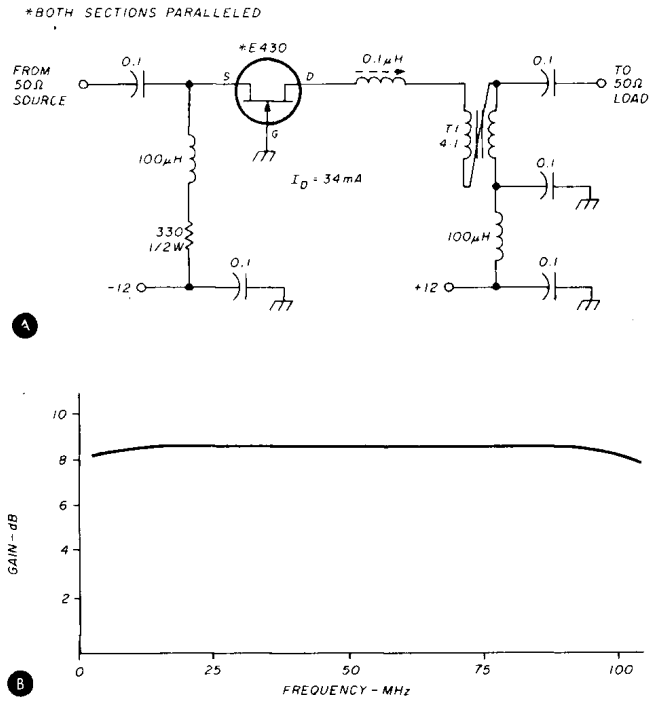

fig. 4. Diagram of the improved broadband jfet amplifier with improved gain, lower noise figure, and better IMD performance. The higher transconductance from the paralleled fets results in a higher gain and better input noise match. Graph (B) shows the overall frequency response of this improved amplifier.

you would have "power match" and best amplifier gain. However, the noise figure in this case could be no better than 3 dB. "Noise match" (optimum drive source impedance for best noise figure) occurs when the driving impedance is considerably higher than the amplifier input impedance. The second point is that although you can specify a 50-ohm output load, the actual output impedance of this amplifier is much higher than 50 ohms (the jfet output is essentially a high-impedance current source). This fact is very important if a filter must follow the amplifier. Where low output VSWR is important, refer to the circuits of **fig. 6** or **7**. All the other circuits in this article have a high output impedance. Finally, the gain of this amplifier is load-sensitive; that is, if the actual value of R_L is greater than 50 ohms, amplifier gain will be higher. Load impedances other than 50 ohms will also require that the value of L_1 be changed for flattest frequency response. If the amplifier is to be used only below 30 MHz, however, L_1 may be omitted entirely. Amplifier gain may vary somewhat depending upon the characteristics of the particular J310 employed. If a negative supply is not available, return R_1 to ground (instead of −12 volts) and select (or adjust) R_1's value for 18 mA of drain current.

improved jfet broadband amplifier

The amplifier shown in **fig. 4A** is very similar to the one just described, but with higher gain, a lower noise figure, and superior IMD performance. **Fig. 4B** shows typical amplifier gain as a function of frequency. Other performance characteristics are as follows:

1 dB gain compression level	+ 14 dBm
2nd-order intercept point	+ 38 dBm
3rd-order intercept point	+ 29 dBm
30-MHz noise figure	<2.5 dB
input VSWR	1.8:1 from 1.8-200 MHz
reverse isolation	36 dB or better to 30 MHz
	30 dB or better to 175 MHz

This amplifier employs the E430 dual jfet as the active device, with individual sections connected directly in parallel (source 1 tied to source 2, gate 1 tied to gate 2, and drain 1 tied to drain 2) to achieve an equivalent ultra-high transconductance jfet. The higher transconductance (≈36,000 micromhos) accounts for the higher gain of this amplifier as compared with that of **fig. 3**. This higher conductance also causes the input impedance to drop to approximately 28 ohms, which accounts for the 1.8:1 input VSWR. Although you no longer have an optimum input power match you're now much closer to an optimum input noise match, which accounts for the improved noise figure. As far as improved IMD performance is concerned, the easiest way to rationalize

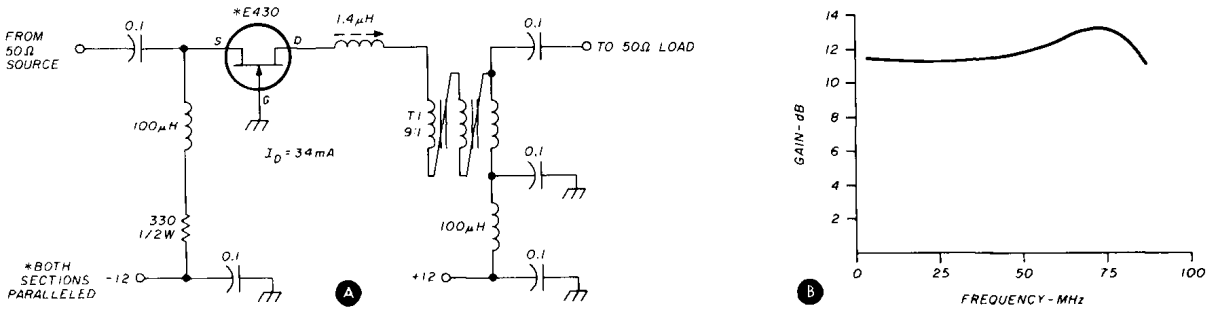

fig. 5. Schematic of a jfet amplifier which exhibits approximately 12 dB gain, though with a narrower bandwidth. In this case, the bandwidth has been sacrificed to produce the higher gain. A plot of the gain vs frequency is shown in (B).

that is to simply say that two devices are carrying the load instead of just one (keeping in mind that you now effectively have two J310s in parallel).

The same considerations with regard to load sensitivity, device variations, and output VSWR are equal-

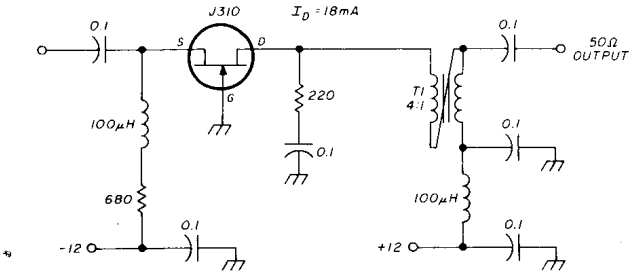

fig. 6. Schematic of a broadband 50-ohm driver where the output impedance is set to 50 ohms. In this case, the 220-ohm resistor loads the collector, leading to the 50-ohm output through the transformer. Gain in this example is approximately unity.

ly applicable to this amplifier as to the one in **fig. 3**. Again, for operation below 30 MHz, peaking inductor L_1 may be omitted. Since the E430 gets quite warm with 34 mA of drain current, it would probably be a good idea to use a heatsink. T_1 is the same 4:1 bifilar-wound transformer as the one shown in **fig. 3**.

higher-gain jfet broadband amplifier

From **eq. 4**, you know that amplifier gain can be increased by raising the effective drain load impedance as seen by the jfet. Therefore, if you replace the 4:1 autotransformer of **fig. 4A** with a 9:1 autotransformer, gain should increase. **Eq. 7**, however, tells you that this will also decrease the bandwidth. Since the amplifier of **fig. 4A** has a bandwidth in excess of 100 MHz, you probably can trade off some of this bandwidth for higher gain in many applications. **Fig. 5A** shows the circuit for such an amplifier. **Fig. 5B** shows the gain as a function of frequency. As predicted, gain has increased at the expense of bandwidth. Other performance characteristics are as follows:

1 dB gain compression level	+ 10 dBm
2nd-order intercept point	+ 36 dBm
3rd-order intercept point	+ 24 dBm
30-MHz noise figure	<2.5 dB
input VSWR	1.6:1 from 1.8-100 MHz
reverse isolation	34 dB or better to 100 MHz

Winding details of the 9:1 autotransformer are presented later in this article. L1 cannot be omitted from this circuit for high-frequency operation unless substantial gain roll off (2-3 dB at 30 MHz) can be tolerated.

jfet broadband drivers

There may be occasions where a better-defined amplifier output impedance is required. **Fig. 6** illustrates a broadband driver circuit designed to present nominal 50-ohm impedances to both the source and load. Since this driver produces somewhat less than unity gain, it is intended only to follow one of the previously discussed amplifiers rather than to stand alone. The circuit is nearly identical to the "basic" jfet broadband amplifier of **fig. 3**. Notice, however, that the drain is ac loaded by a 220-ohm resistor to establish the amplifier output impedance (at the autotransformer output) near 50 ohms. This reduces the gain for two reasons. First, you have lowered the impedance as seen by the J310 drain by a factor of two, thus reducing voltage and power gain by the same factor. Additionally, half the output power is now consumed in the 220-ohm resistor. Thus, the power available to the load is cut by a total factor of 4, or 6 dB. The measured gain of this amplifier is − 1 to − 2 dB from 1.8 to 100 MHz, or 6 to 7 dB lower than that of the "basic" jfet broadband amplifier of **fig. 3**. Other performance characteristics are as follows:

1 dB gain compression level	+ 13 dBm
2nd-order intercept point	+ 36 dBm
3rd-order intercept point	+ 24 dBm
30-MHz noise figure	4-5 dB (estimated)
input VSWR	1.3:1 from 1.8-100 MHz
output VSWR	1.3:1 from 1.8-100 MHz
reverse isolation	35 dB or better to 100 MHz

Fig. 7 shows another broadband driver circuit

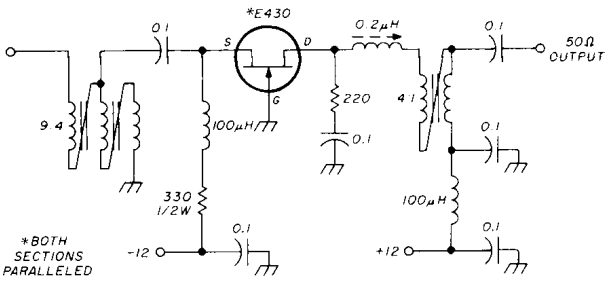

fig. 7. Schematic diagram of another broadband 50-ohm driver which has the input impedance matched by the 9:4 transformer. The gain, in this case, is 1-2 dB.

which provides some gain rather than loss. It is very similar to the "improved" jfet broadband amplifier of **fig. 4A**. Again, the drain is ac loaded by a 220-ohm resistor to establish the amplifier output impedance. Also, the input signal is impedance matched to the jfet source through a 9:4 autotransformer. This transformer is wound identically to the 9:1 autotransformer employed in the "higher gain" jfet broadband amplifier of **fig. 5A**, but is turned "upside-down" to

provide a 9:4 impedance ratio. The gain of this amplifier is 1-2 dB from 1.8-100 MHz. Other performance characteristics are as follows:

1 dB gain compression level	+14 dBm
2nd-order intercept point	+30 dBm
3rd-order intercept point	+29 dBm
30-MHz noise figure	4-5 dB (estimated)
input VSWR	1.3:1 to 30 MHz
	1.8:1 to 100 MHz
output VSWR	1.3:1 to 30 MHz
	1.6:1 to 100 MHz
reverse isolation	40 dB or better to 100 MHz

In both driver circuits, it is important to connect the 220-ohm resistor as closely as possible to the jfet drain with very short lead lengths. If this is not done, oscillations may occur.

winding the autotransformers

The 4:1 autotransformer consists of five turns of bifilar-wound wire on a single-hole ferrite bead. The bifilar wire is made by paralleling and twisting together two dissimilar colored (red and green, for example) of strands of no. 32 AWG (0.2-mm) magnet wire. This is easily done by attaching one end of the paralleled wires in a vice and placing the other end in the chuck of a portable power drill. Maintaining suitable tension on the wires, turn on the drill until the wires have twisted together. Four twists per centimeter (10 twists/inch) is suitable, but this is not at all critical. The only real requirement is that there be enough twists to prevent unraveling but not so many as to cause kinking. The ferrite bead is an FB 43-801. To wind the transformer, wind the bifilar wire through the bead five times, keeping the winding tight to the core. This will result in four strands of bifilar wire against the outside of the bead. Cut off the excess wire, leaving 2-3 cm (approximately 1 inch) or so at each end. Untwist the two ends and bend the green wire of either end and the red wire of the other end toward each other until they meet halfway along the outside wall of the bead, completing the fifth turn. Tin and twist these wires together. Similarly, tin the remaining red and green wire ends. The net result is that the red and green wires are connected *series-aiding*, with their junction being the autotransformer center tap. This 2:1 turns ratio yields a 4:1 impedance ratio. **Fig. 8A** shows an outline drawing of the completed autotransformer along with the corresponding schematic representation.

The 9:1 autotransformer is constructed on the same type of ferrite bead as the 4:1 autotransformer, but is wound with no. 32 AWG (0.2-mm) trifilar wire. The trifilar wire consists of three colored strands, (red, gold, and green, for example) of no. 32 AWG (0.2-mm) wire twisted together in the same manner as the bifilar wire. Wind five turns of the trifilar wire through the ferrite bead and connect the wires series-aiding (see **fig. 8B**). If the input signal and ground connections are reversed, the 9:1 autotransformer then becomes a 9:4 autotransformer.

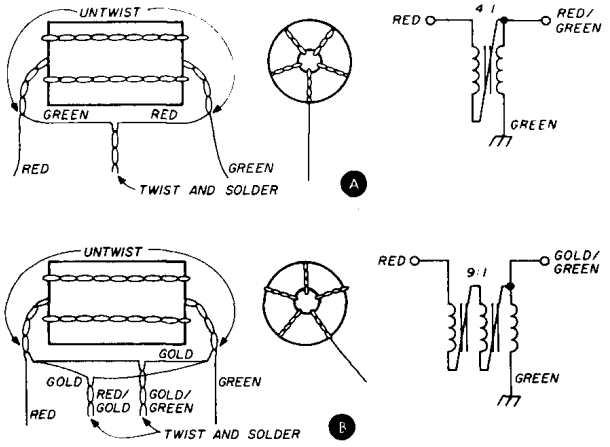

fig. 8. Winding information for the 4:1 and 9:1 transformers. Each transformer uses a ferrite bead, FB 43-801, as the core.

Although the FB 43-801 beads are satisfactory in broadband autotransformer applications, they were selected primarily on the basis of their availability to Amateurs rather than for optimum performance. Two-hole balun cores seem to perform somewhat better.

The FB 43-801 beads may also be used to construct the rf chokes. The 100-μH rf chokes used in the broadband amplifiers may be constructed by winding nine turns of no. 28 AWG (0.3-mm) wire through the beads.

measurement procedures

Swept gain, VSWR, and reverse isolation measurements were made using a Wiltron Model 640 RF analyzer. Noise-figure measurements were made using a calibrated temperature-limited diode-noise generator, a 6-dB pad, a broadband Avantek amplifier, a Heath SB-303 receiver, and an RMS ac VTVM as shown in **fig. 9A**. The noise factor of the pad/amplifier/receiver combination was first measured. The jfet amplifier under test was then inserted between the noise generator and the 6-dB pad, after which the overall system noise factor was measured. The noise factor of the jfet amplifier alone was then calculated using the well-known gain-noise factor equation in rearranged form:

$$F_1 = F_T - \frac{F_2 - 1}{G_1} \qquad (8)$$

where F_1 is the noise factor of the jfet amplifier
F_2 is the noise factor of the pad/amplifier/receiver combination

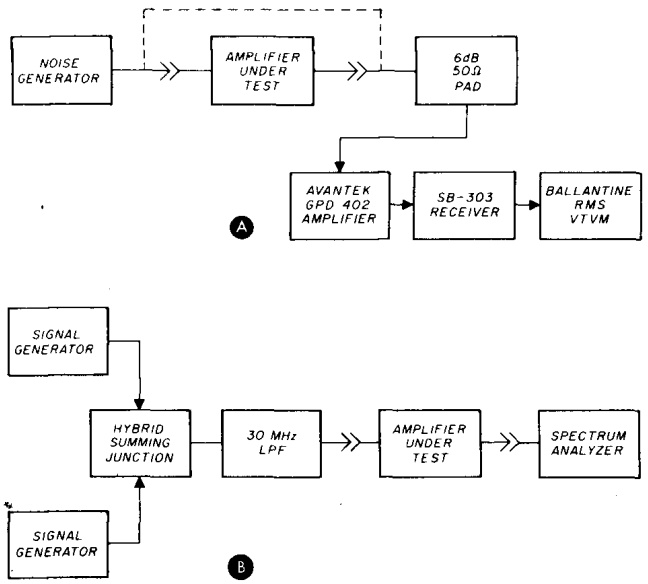

fig. 9. Test setup for the noise-figure and IMD measurements.

G_1 is the power gain factor of the jfet amplifier

F_T is the overall system noise factor

The noise *figure* is then simply 10 $\log_{10}$ noise factor.

Gain compression level measurements were made with an HP-8654B signal generator and an HP-8558B spectrum analyzer. Intercept point measurements were conducted using two HP-8645B signal generators, a 3-dB hybrid junction, a 30-MHz lowpass filter, and an HP-8558B spectrum analyzer. **Fig. 9B** shows the test setup. Second-order intercept point measurements were made by first setting the signal generator outputs to +3.5 dBm (or 0 dBm input to the amplifier after accounting for the 3.5-dB loss at the hybrid junction) at frequencies of 14 and 15 MHz. The difference in amplitude between the 14/15 MHz signal levels and the 29-MHz sum product as observed on the spectrum analyzer was then added to the 0 dBm 14/15 MHz amplifier input signal level to compute the sum product second-order intercept point. The signal generators were then tuned to 27/30 MHz, and the second-order intercept point was again calculated, this time for the 3-MHz difference product. The amplifier second-order intercept point (referenced to the amplifier input) was then taken as the lesser of the two measurements.

Third-order intercept measurements were accomplished by again setting the signal generators to 14/15 MHz at 0 dBm input levels to the amplifier under test. Third-order intermodulation products appeared at 13 and 16 MHz. The difference in amplitude between the 14/15 MHz signals and the greater of the intermodulation products was divided by two and added to 0 dBm to arrive at the third-order intercept point (referenced to the amplifier input).

summary and conclusion

Broadband amplifiers for receiving applications require superior odd- and even-order intermodulation performance due to their greater bandwidths. Jfets make excellent low-noise broadband amplifiers in the high frequency and low vhf range, providing moderate gain and unsurpassed third-order intermodulation performance for the amount of current drawn. Second-order intermodulation performance is good, but may not be as good as that of certain bipolar transistors, particularly when these bipolar transistors are connected in push-pull.[6]

Other devices for consideration as low-noise broadband high-intercept point amplifiers include the Siliconix VMOS[7] and the Signetics DMOS fets.[8] The VMOS fets are capable of performance superior to that of E430s in terms of gain, bandwidth, and dynamic range. To secure maximum gain and linearity, however, it is necessary to run hundreds of milliamperes of current through the device, impractical for most receiving applications. A test of a Siliconix VN33AK VMOS fet at 50 mA of drain current (in the device square-law region) resulted in significantly poorer bandwidth and dynamic range than that of an E430 running at 34 mA. A test of the Signetics SD202 DMOS fet at 20 mA of drain current resulted in a gain somewhat greater than that of a J310 and a third-order intercept point comparable to that of an E430. The extremely low output capacitance of the SD202 resulted in improved bandwidth as well.

Both VMOS and DMOS fets characterized for rf applications are still rather expensive, but both technologies are rapidly advancing in terms of performance and manufacturability. As a result, prices are certain to come down while performance improves (some Siliconix VMOS fets characterized for switching applications already sell for under one dollar in large quantities). In the months ahead, we undoubtedly can look forward to exciting developments in both of these expanding technologies.

references

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